

REMARKS

I. STATUS OF THE APPLICATION

Claims 1-8 are pending in the application.

Claims 1 and 5 stand rejected under 35 U.S.C. §102(b).

Claims 2-4, and 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including the base claim and any intervening claims.

Claim 1 is the only independent claim.

II. AMENDMENTS

The specification has been amended to correct minor grammatical and typographical errors.

Applicants urge that no new matter has been added.

III. CLAIMS 1 AND 5 ARE NOVEL WITHIN THE MEANING OF 35 U.S.C. § 102(b) OVER SNYDER BECAUSE THE APPLIED PRIOR ART FAILS TO TEACH USING A DIGITAL DIFFERENTIAL ANALYZER TO GENERATE A SYNCHRONIZATION SIGNAL

Claims 1 and 5 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Snyder, as described in paragraph 3 of the Office Action, in the following manner:

Consider claims 1 and 5, Snyder recites a system for synchronizing data between two devices operating at different clock frequencies comprising; receiving the data stream at a rate of the first clock, loading (sequentially) the data stream into a plurality of registers at a first clock rate (14, 16); a control circuitry (34) which generates a synchronization signal having a frequency proportional to a ratio of the first clock rate and a second clock (See abstract); reading the plurality of registers at a rate corresponding to the frequency of the synchronization signal. (See abstract,

summary of the invention, col. 3, line 42 to col. 4, lines 21 and col. 5, line 4 to col. 6, line 43).

Applicants respectfully traverse the rejection of claims 1 and 5 under 35 U.S.C. § 102(b) for the following reasons.

Independent claim 1 recites, inter alia,

utilizing a digital differential analyzer to generate a synchronization signal having a frequency proportional to a ratio of said first clock rate and a rate of a second clock.

As described in the specification, for example, on page 11, line 5 through page 12, line 2, the digital differential analyzer generates a synchronization signal, and functions to spread the N words of data as evenly as possible over M clock cycles.

Snyder fails to teach at least the above-identified limitation. Snyder teaches a system wherein a data processor communicates with address and data busses **without any synchronizing methods or systems**. As described in column 4, lines 20-46, the signal asserted on any respective bus will be latched by the data processor at the next occurrence of the next particular edge transition when the data processor and the bus operate at the same frequency. Therefore, Snyder does not teach a synchronization signal. More particularly, Snyder does not teach a digital differential analyzer that generates a synchronization signal having a frequency proportional to a ratio of a first clock rate and a second clock rate.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is clear that Snyder does not anticipate claim 1.

Furthermore, since claim 5 is dependent upon claim 1, and therefore includes all the limitations thereof, Applicants submit that claim 5 additionally is not anticipated by Snyder.

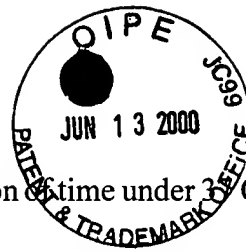
In view of the above remarks, Applicants respectfully submit that claim 1 is not anticipated by Snyder, and urge that the rejection of claim 1, and its dependent claim 5, under 35 U.S.C. § 102(b) be withdrawn.

IV. CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

09/017,224



To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

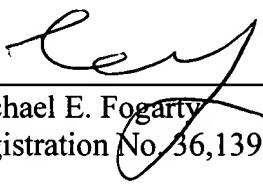
Respectfully submitted,

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